// code design here

module ADDER (a, b, c\_in, sum, c\_out);

input a;

input b;

input c\_in;

output sum;

output c\_out;

assign c\_out = (a & b) | (a & c\_in) | (b & c\_in);

assign sum = a ^ b ^ c\_in;

endmodule

//code testbench here

module test;

reg a;

reg b;

reg c\_in;

wire sum;

wire c\_out;

ADDER adder(a, b, c\_in, sum, c\_out);

initial begin

// Dump waves

$dumpfile("dump.vcd");

$dumpvars(1);

for (int i = 0; i < 8; i++) begin

{a, b, c\_in} = i;

display;

end

end

task display;

#1;

$display("%b + %b + %b = %b%b", a, b, c\_in, c\_out, sum);

endtask

endmodule